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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,574	02/23/2004	Gopal Venkatesan	BP3096	9583
34399 7590 08/04/2008 GARLICK HARRISON & MARKISON P.O. BOX 160727 AUSTIN, TX 78716-0727				
EXAMINER KURR, JASON RICHARD				
ART UNIT 2615		PAPER NUMBER		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/784,574

Applicant(s)

VENKATESAN ET AL.

Examiner

JASON R. KURR

Art Unit

2615

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 April 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SF/ICE)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanna (US 5,796,842) in view of Lee et al (US 6,426,977 B1).

With respect to claim 1, Hanna discloses a digital integrated circuit BTSC signal encoder for encoding audio signals, comprising: (A) a higher order IIR digital filter (fig.3 #224,238, fig.4A, col.11 ln.11-23, 47-49); (B) matrix means (fig.3 #210) for receiving a digital left channel audio signal and a digital right channel audio signal, comprising means for summing (fig.3 #216) said digital left and right channel audio signals and thereby generating a digital sum signal, and including means for subtracting (fig.3 #218) one of said digital left and right channel audio signals from the other of said digital left and right channel audio signals and thereby generating a digital difference signal (col.9 ln.46-63); (C) sum channel processing means (fig.3 #220) for processing said digital sum signal (col.10 ln.20-27); and (D) difference channel processing means (fig.3 #230) for digitally processing said digital difference signal (col.11 ln.24-26).

Hanna does not disclose expressly wherein the higher order IIR digital filter is implemented using an allpass decomposition architecture such that the IIR digital filter, matrix means, sum channel processing means and the difference channel processing means operate at a first sample rate to substantially match BTSC analog filter transform functions in both magnitude and phase.

Lee discloses an apparatus and method for encoding a signal prior to transmission, wherein an allpass decomposition structure (fig.13a) is realized by an IIR digital filter (col.16 ln.51 – col.18 ln.12) such that a first sample rate is achieved to match the sample rate of a related decoder (col.2 ln.17-33). At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the cascaded allpass filters of Lee to implement the high order IIR filters (fig.10 #224,238) of Hanna. The motivation for doing so would have been to provide a BTSC system where synchronization between the encoders and decoders is not needed due to the matched sample rates of an encoding IIR filter and a corresponding decoding FIR filter.

With respect to claim 3, Hanna discloses the BTSC signal encoder of claim 1, wherein the higher order IIR digital filter comprises an input low pass filter (fig.3 #238a, col.11 ln.43-49).

With respect to claim 4, Hanna discloses the BTSC signal encoder of claim 1, wherein the higher order IIR digital filter comprises an output low pass filter (fig.3 #238b, col.11 ln.43-49).

With respect to claim 5, Hanna discloses the BTSC signal encoder of claim 1, wherein the higher order IIR digital filter comprises a sum of multiple cascades of lower order allpass filters (Lee: fig.13).

With respect to claim 6, Hanna discloses the BTSC signal encoder of claim 5, wherein each cascade of lower order allpass filters comprises first or second order allpass filter (Lee: col.5 ln.12-15).

With respect to claim 8, Hanna discloses the BTSC signal encoder of claim 1, wherein the higher order IIR digital filter comprises a pre-emphasis filter in the BTSC encoder (fig.3 #22, col.10 ln.28-42).

With respect to claim 9, Hanna discloses the BTSC signal encoder of claim 1, wherein the higher order IIR digital filter comprises a bandpass filter in the BTSC encoder (fig.3 #280, fig.5 #448, col.13 ln.7-19).

With respect to claim 10, Hanna discloses the BTSC signal encoder of claim 1, wherein the higher order IIR digital filter comprises a variable emphasis compander filter in the BTSC encoder (fig.3 #290, fig.6 #290, col.14 ln.51-55, col.15 ln.53-62).

With respect to claim 11, Hanna discloses an integrated circuit digital BTSC encoder (fig.3) that is operable to encode first and second digital audio signals (fig.3 "L,R") into a BTSC encoded signal comprising (a) a sum channel processor (fig.3 #220) comprising a first digital filter for digitally processing a digital sum signal (col.10 ln.20-27) and (b) a difference channel processor (fig.3 #230) comprising a second digital filter for digitally processing a digital difference signal (col.11 ln.24-26), comprising: a higher order digital filter for filtering a digital audio signal as part of the BTSC encoding process

(col.11 ln.11-23, col.11 ln.47-49); wherein the digital BTSC encoder operates at a sample rate of at least approximately 150-200 kHz so that said digital filters in the sum channel processor and the difference channel processor substantially match BTSC analog filter transform functions in both magnitude and phase (col.19 ln.35-61).

Hanna does not disclose expressly wherein the higher order IIR digital filter is comprised of a cascade of lower order allpass filters.

Lee discloses an apparatus and method for encoding a signal prior to transmission, wherein a cascade of lower order allpass filters (fig.13a) is realized by an IIR digital filter (col.16 ln.51 – col.18 ln.12) such that a first sample rate is achieved to match the sample rate of a related decoder (col.2 ln.17-33). At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the cascaded allpass filters of Lee to implement the high order IIR filters (fig.10 #224,238) of Hanna. The motivation for doing so would have been to provide a BTSC system where synchronization between the encoders and decoders is not needed due to the matched sample rates of an encoding IIR filter and a corresponding decoding FIR filter.

With respect to claim 13, Hanna discloses the integrated circuit digital BTSC encoder of claim 11, wherein the higher order digital filter comprises a sum of multiple cascades of lower order allpass filters (Lee: fig.13).

With respect to claim 14, Hanna discloses the integrated circuit digital BTSC encoder of claim 11, however does not disclose expressly wherein the higher order IIR digital filter comprises an eleventh order Caue low pass filter IIR. Official Notice is taken that Caue filters are well known in the art to be implemented within digital

impulse filtering systems. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a Causer filter as the Infinite Impulse Response filter of Hanna. The motivation for doing so would have been to use readily available digital processing techniques to realize the desired filtering of Hannah. Hanna discloses wherein the IIR filter (fig.3 #224) is of the tenth order (col.11 ln.10-23), and wherein the EQ filter (fig.3 #228) is a first order all-pass filter (col.10 ln.49-58). At the time of the invention it would have been obvious to a person of ordinary skill in the art that multiple filters such as filters #224 and #228 may be realized by the same IIR filter, resulting in an eleventh order IIR filter. The motivation for implementing multiple filters on a single digital filter would have been to reduce the size and cost of the encoding system.

With respect to claim 15, Hanna discloses the integrated circuit digital BTSC encoder of claim 14, wherein the cascade of lower order allpass filters comprises a first order allpass filter (col.10 ln.49-58) and a plurality of second order allpass filters (col.11 ln.10-23).

With respect to claim 17, Hanna discloses the integrated circuit digital BTSC encoder of claim 11, wherein the sum channel processor, difference channel processor and higher order digital filter are fabricated on a single silicon substrate using CMOS processing (col.18 ln.20-34).

With respect to claim 18, Hanna discloses the integrated circuit digital BTSC encoder of claim 11, wherein the higher order digital filter comprises a pre-emphasis filter in the BTSC encoder (fig.3 #222, col.10 ln.28-42).

With respect to claim 19, Hanna discloses the integrated circuit digital BTSC encoder of claim 11, wherein the higher order digital filter comprises a bandpass filter in the BTSC encoder (fig.3 #290, fig.6 #290, col.14 ln.51-55, col.15 ln.53-62).

With respect to claim 20, Hanna discloses a single chip set top box integrated circuit digital BTSC encoder (fig.3, col.18 ln.20-34) that is operable to encode first and second digital audio signals (fig.3 "L,R") into a BTSC encoded signal, comprising a higher order IIR filter.

Hanna does not disclose expressly wherein the higher order IIR filter is implemented using an allpass decomposition filter structure comprising a sum of two allpass filter stages, where each allpass filter stage comprises a plurality of lower order allpass IIR filters.

Lee discloses an apparatus and method for encoding a signal prior to transmission, wherein a sum of two allpass filters stages (fig.13a), where each allpass filter stage comprises a plurality of lower order allpass IIR filters (fig.13b,c) is realized by an IIR digital filter (col.16 ln.51 – col.18 ln.12) such that a first sample rate is achieved to match the sample rate of a related decoder (col.2 ln.17-33). At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the cascaded allpass filters of Lee to implement the high order IIR filters (fig.10 #224,238) of Hanna. The motivation for doing so would have been to provide a BTSC system where synchronization between the encoders and decoders is not needed due to the matched sample rates of an encoding IIR filter and a corresponding decoding FIR filter.

With respect to claim 21, Hanna discloses the digital BTSC encoder of claims 20, where in the lower order allpass IIR filters comprise a first or second order allpass filter (Lee: col.5 ln.12-15).

With respect to claims 2, 7, 12 and 16, Hanna discloses the BTSC signal encoder of claim 1 and 11 respectively, however does not disclose expressly wherein the higher order IIR digital filter comprises a Cauer low pass filter or a Butterworth low pass filter. Official Notice is taken that Cauer and Butterworth filters are well known in the art to be implemented within digital impulse filtering systems. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a Cauer or Butterworth filter as the Infinite Impulse Response filter of Hanna. The motivation for doing so would have been to use readily available digital processing techniques to realize the desired filtering of Hannah.

Response to Arguments

Applicant's arguments, see "Remarks", filed April 10, 2008, with respect to the rejection(s) of claim(s) 1-21 under Hanna (US 5,796,842) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Lee et al (US 6,426,977 B1).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON R. KURR whose telephone number is (571)272-0552. The examiner can normally be reached on M-F 10:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin can be reached on (571) 273-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason R Kurr/
Examiner, Art Unit 2615

/Vivian Chin/
Supervisory Patent Examiner, Art Unit 2615